CLAIMS

1. A memory hub for a hub-based memory module, comprising:

first and second link interfaces for coupling to respective data busses;

a data path coupled to the first and second link interfaces and through which data is transferred between the first and second link interfaces; and

a write bypass circuit coupled to the data path to couple write data on the data path and temporarily store the write data to allow read data to be transferred through the data path while the write data is temporarily stored.

2. The memory hub of claim 1 wherein the write bypass circuit comprises:

a multiplexer having a first input coupled to the data path and further having a second input, an output, and a selection terminal, the multiplexer coupling the output to the first or second input in accordance with a selection signal applied to the selection terminal;

a first-in-first-out (FIFO) register having an input coupled to the data path and further having an output coupled to the second input of the multiplexer;

an output buffer having a buffer input coupled to the output of the multiplexer and further having a buffer output and an activation terminal, the output buffer coupling the buffer input to the buffer output in accordance with an activation signal applied to the activation terminal; and

a selection circuit coupled to the multiplexer to generate the selection signal and activation signal when activated to couple the second input of the multiplexer to the output of the multiplexer.

3. The memory hub of claim 2 wherein the write bypass circuit further comprises an input buffer having an input coupled to the data path and an output coupled to the inputs of the multiplexer and the FIFO register.

4. The memory hub of claim 1, further comprising a memory device interface coupled to the data path, the memory device interface for coupling data to at least one memory device to which the memory device interface can be coupled.

5. A memory hub for a hub-based memory module, comprising:

a first link interface for coupling to a first data bus to provide data to the first data bus and receive data from the first data bus;

a second link interface for coupling to a second data bus to provided data to the second data bus and receive data from the second data bus;

a switching circuit coupled to the first and second link interfaces to couple data between the first and second link interfaces; and

a data bypass circuit coupled to the switching circuit to store a first set of data received by either the first or second link interfaces to allow a second set of data to be coupled between the first and second link interfaces without interference by the first set of data.

6. The memory hub of claim 5 wherein the data bypass circuit comprises:

a multiplexer having a first input coupled to the switching circuit and further having a second input, an output, and a selection terminal, the multiplexer coupling the output to the first or second input in accordance with a selection signal applied to the selection terminal;

a first-in-first-out (FIFO) register having an input coupled to the switching circuit and further having an output coupled to the second input of the multiplexer;

an output buffer having a buffer input coupled to the output of the multiplexer and further having a buffer output and an activation terminal, the output buffer coupling the buffer input to the buffer output in accordance with an activation signal applied to the activation terminal; and

a selection circuit coupled to the multiplexer to generate the selection signal and activation signal when activated to couple the second input of the multiplexer to the output of the multiplexer.

7. The memory hub of claim 6 wherein the data bypass circuit further comprises an input buffer having an input coupled to the switching circuit and an output coupled to the inputs of the multiplexer and the FIFO register.

8. The memory hub of claim 5, further comprising a memory device interface coupled to the switching circuit, the memory device interface for coupling data to at least one memory device to which the memory device interface can be coupled.

9. The memory hub of claim 8 wherein the memory device interface comprises:

a memory controller coupled to the data path through a memory controller bus and further having a memory device terminal to which a memory device can be coupled;

a write buffer coupled to the memory controller for storing memory requests; and

a cache coupled to the memory controller for storing data.

10. The memory hub of claim 5 wherein the first set of data represents write data and the second set of data represents read data.

11. A memory module, comprising:

a plurality of memory devices; and

a memory hub coupled to the plurality of memory devices, the memory hub comprising:

first and second link interfaces for coupling to respective data busses;

a data path coupled to the first and second link interfaces and through which data is transferred between the first and second link interfaces; and

a write bypass circuit coupled to the data path to couple write data on the data path and temporarily store the write data to allow read data to be transferred through the data path while the write data is temporarily stored.

12. The memory module of claim 11 wherein the write bypass circuit of the memory hub comprises:

a multiplexer having a first input coupled to the data path and further having a second input, an output, and a selection terminal, the multiplexer coupling the output to the first or second input in accordance with a selection signal applied to the selection terminal;

a first-in-first-out (FIFO) register having an input coupled to the data path and further having an output coupled to the second input of the multiplexer;

an output buffer having a buffer input coupled to the output of the multiplexer and further having a buffer output and an activation terminal, the output buffer coupling the buffer input to the buffer output in accordance with an activation signal applied to the activation terminal; and

a selection circuit coupled to the multiplexer to generate the selection signal and activation signal when activated to couple the second input of the multiplexer to the output of the multiplexer.

13. The memory module of claim 12 wherein the write bypass circuit of the memory hub further comprises an input buffer having an input coupled to the data path and an output coupled to the inputs of the multiplexer and the FIFO register.

14. The memory module of claim 11 wherein the memory hub further comprises a memory device interface coupled to the data path and to at least one of the plurality of memory devices, the memory device interface for coupling data to the memory device.

15. The memory module of claim 14 wherein the memory device interface of the memory hub comprises:

a memory controller coupled to the data path through a memory controller bus and further coupled to at least one of the plurality of memory devices through a memory device bus;

a write buffer coupled to the memory controller for storing memory requests directed to the memory device coupled to the memory controller; and

a cache coupled to the memory controller for storing data provided to the memory device or retrieved from the memory device.

16. A memory module, comprising:

a plurality of memory devices; and

a memory hub coupled to at least one of the plurality of memory devices, the memory hub comprising:

a first link interface for coupling to a first data bus to provide data to the first data bus and receive data from the first data bus;

a second link interface for coupling to a second data bus to provided data to the second data bus and receive data from the second data bus;

a switching circuit coupled to the first and second link interfaces to couple data between the first and second link interfaces; and

a data bypass circuit coupled to the switching circuit to store a first set of data received by either the first or second link interfaces to allow a second set of data to be coupled between the first and second link interfaces without interference by the first set of data.

17. The memory module of claim 16 wherein the data bypass circuit of the memory hub comprises:

a multiplexer having a first input coupled to the switching circuit and further having a second input, an output, and a selection terminal, the multiplexer coupling the output to the first or second input in accordance with a selection signal applied to the selection terminal;

a first-in-first-out (FIFO) register having an input coupled to the switching circuit and further having an output coupled to the second input of the multiplexer;

an output buffer having a buffer input coupled to the output of the multiplexer and further having a buffer output and an activation terminal, the output buffer coupling the buffer

input to the buffer output in accordance with an activation signal applied to the activation terminal; and

a selection circuit coupled to the multiplexer to generate the selection signal and activation signal when activated to couple the second input of the multiplexer to the output of the multiplexer.

18. The memory module of claim 17 wherein the data bypass circuit of the memory hub further comprises an input buffer having an input coupled to the switching circuit and an output coupled to the inputs of the multiplexer and the FIFO register.

19. The memory module of claim 16 wherein the memory hub further comprises a memory device interface coupled to the data path and to at least one of the plurality of memory devices, the memory device interface for coupling data to the memory device.

20. The memory module of claim 16 wherein the first set of data represents write data and the second set of data represents read data.

21. A processor-based system, comprising:

a processor having a processor bus;

a system controller coupled to the processor bus, the system controller having a system memory port and a peripheral device port;

at least one input device coupled to the peripheral device port of the system controller;

at least one output device coupled to the peripheral device port of the system controller;

at least one data storage device coupled to the peripheral device port of the system controller; and

a memory module coupled to the system memory port of the system controller, the memory module comprising:

a plurality of memory devices; and

a memory hub coupled to the plurality of memory devices, the memory hub comprising:

first and second link interfaces for coupling to respective data busses;

a data path coupled to the first and second link interfaces and through which data is transferred between the first and second link interfaces; and

a write bypass circuit coupled to the data path to couple write data on the data path and temporarily store the write data to allow read data to be transferred through the data path while the write data is temporarily stored.

22. The processor-based system of claim 21 wherein the write bypass circuit of the memory hub comprises:

a multiplexer having a first input coupled to the data path and further having a second input, an output, and a selection terminal, the multiplexer coupling the output to the first or second input in accordance with a selection signal applied to the selection terminal;

a first-in-first-out (FIFO) register having an input coupled to the data path and further having an output coupled to the second input of the multiplexer;

an output buffer having a buffer input coupled to the output of the multiplexer and further having a buffer output and an activation terminal, the output buffer coupling the buffer input to the buffer output in accordance with an activation signal applied to the activation terminal; and

a selection circuit coupled to the multiplexer to generate the selection signal and activation signal when activated to couple the second input of the multiplexer to the output of the multiplexer.

23. The processor-based system of claim 22 wherein the write bypass circuit of the memory hub further comprises an input buffer having an input coupled to the data path and an output coupled to the inputs of the multiplexer and the FIFO register.

24. The processor-based system of claim 21 wherein the memory hub further comprises a memory device interface coupled to the data path and to at least one of the plurality of memory devices, the memory device interface for coupling data to the memory device.

25. The processor-based system of claim 24 wherein the memory device interface of the memory hub comprises:

a memory controller coupled to the data path through a memory controller bus and further coupled to at least one of the plurality of memory devices through a memory device bus;

a write buffer coupled to the memory controller for storing memory requests directed to the memory device coupled to the memory controller; and

a cache coupled to the memory controller for storing data provided to the memory device or retrieved from the memory device.

26. A processor-based system, comprising:

a processor having a processor bus;

a system controller coupled to the processor bus, the system controller having a system memory port and a peripheral device port;

at least one input device coupled to the peripheral device port of the system controller;

at least one output device coupled to the peripheral device port of the system controller;

at least one data storage device coupled to the peripheral device port of the system controller; and

a memory module coupled to the system memory port of the system controller, the memory module comprising:

a plurality of memory devices; and

a memory hub coupled to at least one of the plurality of memory devices, the memory hub comprising:

a first link interface for coupling to a first data bus to provide data to the first data bus and receive data from the first data bus;

a second link interface for coupling to a second data bus to provided data to the second data bus and receive data from the second data bus;

a switching circuit coupled to the first and second link interfaces to couple data between the first and second link interfaces; and

a data bypass circuit coupled to the switching circuit to store a first set of data received by either the first or second link interfaces to allow a second set of data to be coupled between the first and second link interfaces without interference by the first set of data.

27. The processor-based system of claim 26 wherein the data bypass circuit of the memory hub comprises:

a multiplexer having a first input coupled to the switching circuit and further having a second input, an output, and a selection terminal, the multiplexer coupling the output to the first or second input in accordance with a selection signal applied to the selection terminal;

a first-in-first-out (FIFO) register having an input coupled to the switching circuit and further having an output coupled to the second input of the multiplexer;

an output buffer having a buffer input coupled to the output of the multiplexer and further having a buffer output and an activation terminal, the output buffer coupling the buffer input to the buffer output in accordance with an activation signal applied to the activation terminal; and

a selection circuit coupled to the multiplexer to generate the selection signal and activation signal when activated to couple the second input of the multiplexer to the output of the multiplexer.

28. The processor-based system of claim 27 wherein the data bypass circuit of the memory hub further comprises an input buffer having an input coupled to the switching circuit and an output coupled to the inputs of the multiplexer and the FIFO register.

29. The processor-based system of claim 26 wherein the memory hub further comprises a memory device interface coupled to the data path and to at least one of the plurality of memory devices, the memory device interface for coupling data to the memory device.

30. The processor-based system of claim 29 wherein the memory device interface of the memory hub comprises:

a memory controller coupled to the data path through a memory controller bus and further coupled to at least one of the plurality of memory devices through a memory device bus;

a write buffer coupled to the memory controller for storing memory requests directed to the memory device coupled to the memory controller; and

a cache coupled to the memory controller for storing data provided to the memory device or retrieved from the memory device.

31. The processor-based system of claim 26 wherein the first set of data represents write data and the second set of data represents read data.

32. A method for writing data to a memory location in a memory system coupled to a memory bus, comprising:

accessing read data in the memory system;

providing write data to the memory system on the memory bus;

coupling the write data to a register in the memory system for temporary storage of the write data;

coupling the read data to the memory bus and providing the read data for reading;

coupling the write data stored in the register to the memory bus; and

writing the write data to the memory location.

33. The method of claim 32, further comprising issuing a read command to the memory system prior to issuing a write command to the memory system.

34. The method of claim 32 wherein providing the write data to the memory system comprises providing the write data through at least one memory module of the memory system prior to coupling the write data to the register.

35. The method of claim 32 wherein the memory system includes a plurality of memory modules coupled in series on the memory bus, and writing the write data to the memory location comprises writing the write data to a memory location located in a memory module located downstream of the memory module from which the read data was accessed.

36. A method for executing memory commands in a memory system having a memory bus, the method comprising:

issuing a read command to the memory system;

issuing a write command to a memory location in the memory system and providing write data to the memory bus of the memory system;

accessing read data in the memory system;

in the memory system, decoupling the write data from the memory bus;

receiving the read data on the memory bus from the memory system;

recoupling the write data to the memory bus; and

resuming the write command to the memory location.

37. The method of claim 36 wherein issuing the read command to the memory system precedes issuing the write command to the memory system.

38. The method of claim 36, further comprising temporarily storing the write data in a bypass buffer during the receipt of the read data.

39. The method of claim 36 wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus.

40. A method for executing read and write commands in a memory system having a memory bus, the method comprising:

issuing a read command to access a first memory location in the memory system;

before completion of the read command, scheduling a write command to write data to a second memory location in the memory system

retrieving read data from the first memory location;

providing write data to the memory bus of the memory system;

in the memory system, bypassing the read data on the memory bus;

receiving the read data on the memory bus from the memory system; and

providing the write data to the memory bus.

41. The method of claim 40 wherein bypassing the read data on the memory bus comprises decoupling the write data from the memory bus for a time period to avoid data collision on the memory bus.

42. The method of claim 41, further comprising temporarily storing the write data in a bypass buffer during the receipt of the read data.

43. The method of claim 41 wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus.